A Monolithic Stacked Class-D Approach for High Voltage DC-AC Conversion in Standard CMOS

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***Abstract*— A fully-integrated Class-D DC-AC converter is realized in a 130 nm 1.2V CMOS technology with an on-chip inductor and capacitor. Several dies are combined to achieve higher output power. A multilevel topology allows the combined Class-D DC-AC system to achieve higher output voltages at a multiple of the nominal supply voltage of 1.2V. Problems such as hot carrier degradation and oxide breakdown are absent, since each subblock operates within the standard voltage limits. An off-chip low frequency signal can be used as a reference clock for the Class-D DC-AC converter using an on-chip PWM generation circuit. For this monolithic multilevel system, no discrete components are needed anymore, reducing the bill of materials. A maximum efficiency of 66.5% for a stand-alone die is reached. An output peak voltage of 2.4V peak-to-peak is achieved at an efficiency of 33% by using a combination of several dies. A total output power of 95mW is obtained.**

I. Introduction

In recent years, there has been an enormous increase in the interest for on-chip power conversion techniques from industry. The integration reduces the bill of materials (BOM) for the producer after all. Recent research efforts demonstrated the feasibility of the development of fully-integrated DC-DC converters in standard CMOS technologies [1]. The next leap in this trend is the integration of even more complex power conversion blocks. More specifically: monolithic AC-DC and DC-AC conversion. The main feature of a DC-AC converter, or inverter, exists in converting a DC source into an AC source. The frequency and amplitude of the converter output can be adjusted. Inverters are extensively used in uninterrupted power supplies (UPS), motor drivers, cold cathode fluorescent lamps (CCFL) and photovoltaic (PV) panels. The common output frequency range of these inverters is from 0 to 10 kHz. Present-day commercial inverters are using external components, increasing the BOM. By taking the next leap towards a monolithic integration of inverters, a less expensive solution is achieved. Moreover, this will result in a flexible inverter that can achieve a much wider frequency range. This enables the possibility to control microscale piezoelectric motors and magnetic machines which require high driving frequencies above 100 kHz. On the other hand, the generation of low-frequency signals should remain possible on-chip as well. This is a major challenge as the on-chip passives are inherently small, thus requiring techniques to overcome this issue.

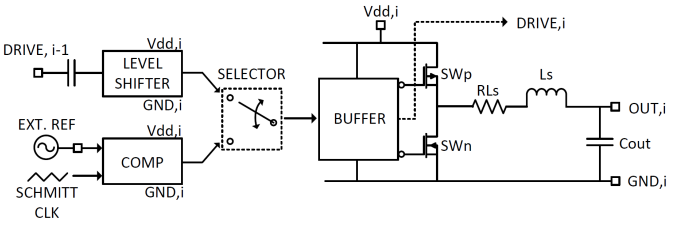


Fig. 1. Overview of a one-stage monolithic class-D DC-AC converter. Small squares indicate bond pads.

A high output voltage will be preferred. In a high-voltage design in standard CMOS technology, breakdown mechanisms and hot carrier effects will be present. Non-standard CMOS technologies, such as DMOS [2], can be used but introduce extra cost. To prevent this problem, in this paper several dies are combined as subblocks of a complete system. Each subblock operates within the nominal $130\ nm$ CMOS voltage limits. In this way, no stress is introduced and high output voltage can be achieved.
This paper presents a stacked class-D approach for monolithic DC-AC conversion. The architecture and operating principles are described in section II. The implementation of the most important components of the stacked class-D converter is discussed in section III. Section IV describes the measurement results. Finally, conclusions are drawn in section V.

II. Architecture

A. One-stage monolithic Class-D DC-AC converter

The designed on-chip system for DC-AC conversion is depicted in Figure 1. On the right hand side, a basic class-D topology is seen. It consists of an on-chip inductor L_S, on-chip combined MOS and MIM capacitor C_{OUT}, two power switches SW_p and SW_n and the needed buffers to drive these. Class D voltage-switching inverters are fed by a DC voltage source V_{dd}. The inductor and capacitor form a series-resonant circuit. If the quality factor is sufficiently high, the current through the resonant circuit is sinusoidal and the currents through the switches are half-wave sinusoids. The voltages across the switches are square waves. This is discussed in detail in previous work of the author [3].

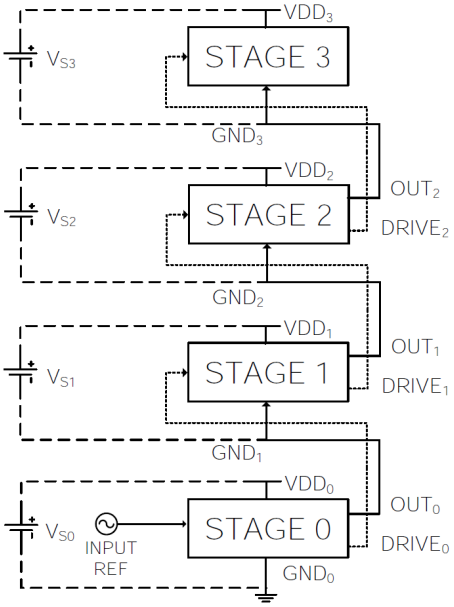


Fig. 2. Block diagram for serialization of several dies.

The left hand side of Figure 1 depicts the PWM (pulse-width modulation) generation circuitry, used to generate the non-overlapping high-frequency clock for the power switches. These clock-pulses are either generated on-chip using a comparator or an off-chip clock signal is brought on-chip using a level shifter. The selector enables one to either choose the off-chip or on-chip generated clock. The different blocks of the clock generation circuit will be discussed in more detail in section III.

B. Multiple stage stacked Class-D DC-AC conversion

The design of the one-stage monolithic class-D DC-AC converter provides the possibility to serialize different systems into a multi-stage or stacked class-D system [4]. This enables a higher output voltage and higher output power, while operating within the nominal voltage limits for the CMOS technology on every single die. This principle is explained in Figure 2 for a combination of four blocks.

Stage 0 is the first stage of the complete stacked solution. An external low-voltage input reference waveform is applied to this first stage (e.g. a 50 Hz sine). Using an on-chip sawtooth waveform, the on-chip comparator can generate the PWM clock waveform needed to drive the class-D power switches. This will be explained in section III. The clock waveform is buffered and applied to the switches. This resulting buffered signal $DRIVE_0$ is brought off-chip as well (see Figure 1). The result is an output sine wave with a frequency equal to the input reference and a peak-to-peak voltage equal to the supply voltage $V_{DD0} = V_{S0}$ for an ideal class-D amplifier [5]. This sinusoidal output waveform OUT_0 can now be used as a ground reference for a second stand-alone die, now called *Stage 1*. One can derive this mathematically as follows:

$$V_{input} = \frac{1}{2} * sin(2\pi f_{ref} t) + \frac{V_{S0}}{2} \tag{1}$$

This input signal is modulated on a high-frequency carrier (see section III). At the output of the Class D DC-AC converter, the low-pass filter of the combined inductor and capacitor has a low cutoff frequency in relation to the switching frequencies. A Fourier analysis indicates that these higher order harmonics can be neglected [6] which yields the following expression for the output voltage:

$$\begin{aligned} OUT_0 &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * VDD_0 \\ &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S0} \end{aligned} \tag{2}$$

The second die has exactly the same system as the first die. However, the clock reference is not generated on-chip, but the second die is now clocked using the $DRIVE_0$ signal generated in Stage 0 as a reference. This $DRIVE_0$ signal is level-shifted in Stage 1 to be between VDD_1 and GND_1. A separate and stand-alone DC source V_{S1} is used as a supply for Stage 1. The GND_1 reference is equal to OUT_0. The output voltage for Stage 1 is:

$$\begin{aligned} OUT_1 &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * (VDD_1 - GND_1) + GND_1 \\ &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * (V_{S1}) + GND_1 \\ &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * (V_{S1}) + OUT_0 \end{aligned} \tag{3}$$

Substituting equation (2) into (3), and taking into account that all independent voltage sources V_{Si} have the same DC voltage yields:

$$\begin{aligned} OUT_1 &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S1} + \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S0} \\ &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_S + \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_S \\ &= V_S + sin(2\pi f_{ref} t) * V_S \\ &= 2 * OUT_0 \end{aligned} \tag{4}$$

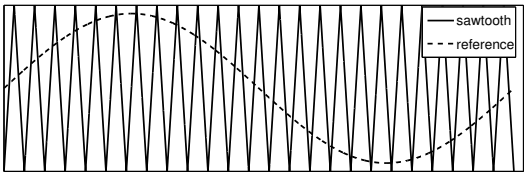
This means that the output voltage amplitude for a combined load over Stage 0 and Stage 1 has now been doubled. This can be extrapolated for the use of multiple stages. Stage i has the following expression for the output voltage over a combined load for Stage 0, Stage 1, ... Stage i-1 and Stage i:

$$OUT_i = i * \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_S \tag{5}$$

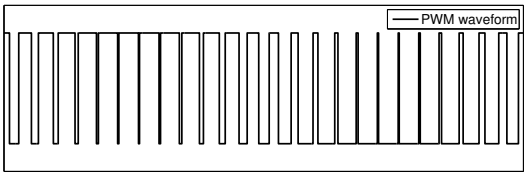
where every stage has the same DC voltage V_S for the independent voltage sources.

III. Implementation

In this section, the implementation of the different blocks for the monolithic class-D DC-AC converter is discussed.



(a) On-chip high frequency sawtooth and external reference as input for the comparator.



(b) PWM waveform as output from comparator.

Fig. 3. PWM generation principle.

A. PWM generation

Since the class-D converter circuit has an on-chip inductor and capacitor with limited sizes due to area-constraints, a high switching frequency is needed to achieve high-efficiency power conversion. Therefore, the PWM generation circuit will need to generate the clock signal for the power switches at a high frequency. For the PWM-generation, an external reference will be compared to an on-chip sawtooth waveform, yielding a PWM waveform at the output of the comparator. This is indicated in Figure 3. The generation of the on-chip sawtooth waveform is achieved using a Schmitt-trigger circuit and an on-chip $1pF$ MIM-capacitor C. The circuit is depicted in Figure 4. The Schmitt-trigger is designed to have a threshold at $300mV$ and $900mV$. The different threshold voltages are reached by dynamically switching transistors M_{1sup} or M_{2sup} using the $CTRL$ signal, based on the idea in [7]. The MIM-capacitor determines the sawtooth frequency. In a first phase, the capacitor will be charged by transistor M_{CRG} until the voltage over the capacitor has reached $900mV$. At this point, transistor M_{CRG} will be switched off and transistor M_{DCRG} will be turned on, discharging the capacitor until the voltage has reached $300mV$. The capacitor will now be charged again. This results in a high frequency sawtooth waveform at the $OUTPUT$ node. For the comparator, a standard symmetrical OTA is used.

B. Level shifter

The level shifter is implemented as shown in Figure 5. An on-chip capacitor C_{level} is used to couple the external drive signal CLK into the selector, so that it can be used as a clock signal. This capacitor is a $5pF$ MIM-capacitor. Since the GND_2 signal will be the output signal of a previous chip, both the GND_2 and Vdd_2 signals will be sinusoidal. The resistor ensures that the DC voltage of the input node is always exactly in between Vdd_2 and GND_2. This is implemented by using an on-chip poly-resistor.

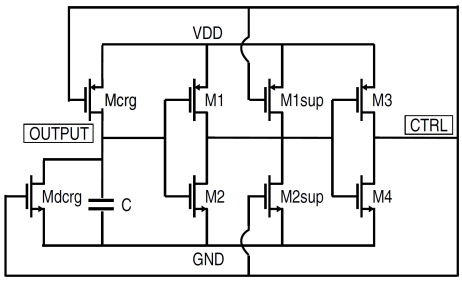


Fig. 4. Circuit for the Schmitt-trigger based sawtooth generator.

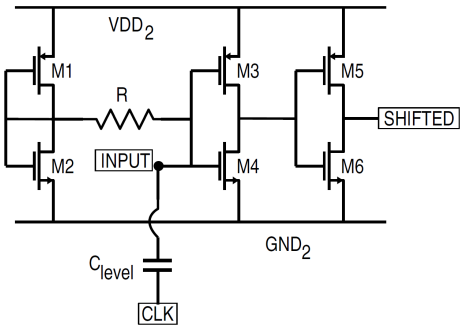


Fig. 5. Circuit for the level shifter.

C. On-chip inductor and capacitor

The on-chip inductor is implemented as an octagonal metal track hollow spiral inductor. It consists of three windings, with a width of $57\mu m$. Several metal layers are used to reduce the parasitic series resistance: standard metal layers, a thick top metal and an aluminum layer. The result is a total inductance of $10nH$ and a parasitic series resistance of 2Ω at a switching frequency of 100MHz. The total area used is $430\mu m$ by $430\mu m$.

The output capacitor is a combination of MOS and MIM capacitors. This is done to achieve the highest possible density. The capacity density for MOSCAP is $10fF/\mu m^2$, for MIMCAP $2fF/\mu m^2$. This is without taking area overhead into account because of the MOS gates or MIMCAP connections. Since the output will swing between GND and VDD, it is necessary to combine a MOSCAP based on pMOS transistors with a MOSCAP based on nMOS transistors. Only then is it possible to achieve an output capacitor that has a fixed value across the complete output swing. The combined pMOS and nMOS capacitor has a capacitance of $1.5nF$, the MIMCAP is $1nF$. The area of the MIMCAP is $1mm^2$ which is much larger than the $0.4mm^2$ of the combined MOSCAP because it can be processed on top of the decoupling capacitance. This yields a total on-chip output capacitance of $2.5nF$.

The power switches SWp and SWn are implemented using a fingered layout. The width of these switches is $3.6mm$ and $1.4mm$. A buffer train is used to apply the non-overlapping clock to the switches.

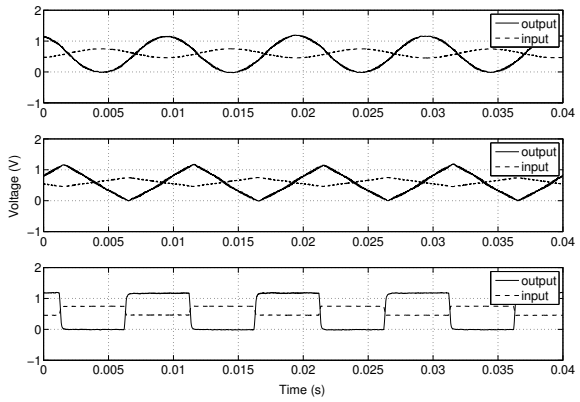


Fig. 6. Measured input and output waveforms using one class-D DC-AC converter.

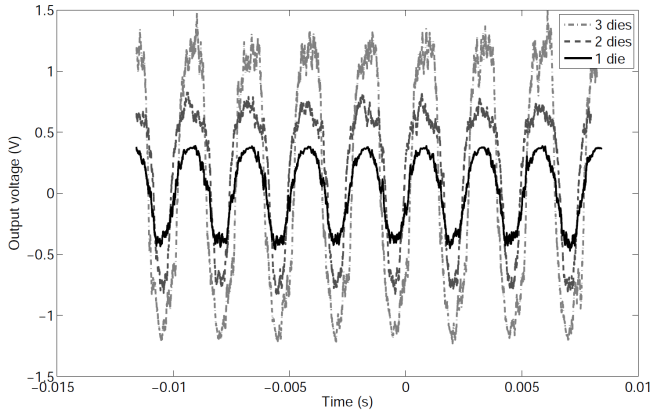


Fig. 7. Output waveforms for 1, 2 and 3 series connected class-D DC-AC converters.

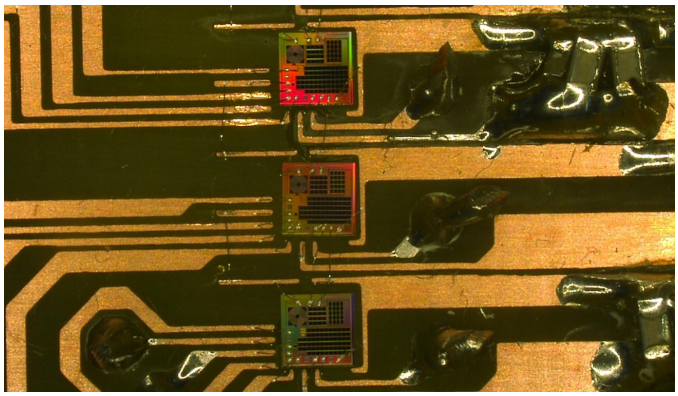


Fig. 8. Three dies, inter-die bonded on a PCB.

IV. Measurements

A monolithic class-D DC-AC converter is implemented in a 130 nm 1.2 V CMOS technology. It measures 1.5 mm x 1.5 mm. Figure 8 shows a die photograph where three dies are connected. Several measurements were performed using one die or more dies. For one stand-alone die, Figure 6 shows the behaviour when either a sine, square or triangle waveform are applied at the input. The maximum efficiency is 66.5% with an output amplitude of $1.03Vpp$, when an input sine is applied at 100Hz for an off-chip load of 30Ω. This yields a total measured output power of 35.1 mW.

Several dies are now connected in a series stacked topology. Figure 7 shows the output waveforms when either one, two or three dies are used. The input reference signal is a sine wave at 400Hz. An off-chip load of 230Ω is used. The output peak amplitude increases from $0.73Vpp$, over $1.7Vpp$ to $2.4Vpp$. Hence, using the series stacking, a higher output voltage can be reached while maintaining operation within the voltage limits for each separate die. The according efficiencies for these cases are 64.3%, 50.1% and 33.2%. It is seen that the efficiencies are dropping when more dies are combined. This is assumed to be caused by parasitics in the measurement setup and test pins. The total output power in each case is 34.1 mW, 46.2 mW and 94.7 mW. The output waveforms are clearly synchronized, as can be seen in Figure 7. This is important, otherwise the signals in two different stages would cancel out. The synchronization is inherently present, since the PWM switching frequency is much higher than the nominal frequencies used in the reference signals.

V. Conclusion

A fully-integrated class-D DC-AC converter is realized in a 130 nm 1.2 V CMOS technology with an on-chip inductor and capacitor. Several dies are combined to achieve a higher output voltage and accordingly higher output power, while using the same standard CMOS technology. A low-frequency off-chip reference signal can be used as a reference to clock the class-D DC-AC converter. Because of the monolithic nature of the system, the bill of materials is heavily reduced. A maximum efficiency of 66.5% is achieved for one stand-alone die. An output peak voltage of 2.4 V peak-to-peak is achieved for a combination of three stacked dies at an efficiency of 33% with a maximal output power of 95 mW.

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